Appl. No. 10/724,863
Response Dated May 15, 2006
Reply to Office Action of February 15, 2006

## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

## Listing of Claims:

1 (Withdrawn).    A method, comprising:

receiving a new store into an instruction window;

storing a previous store into a second level circuit, wherein said second level circuit includes at least one block associated with a checkpoint; and

inserting a subsequent store into said instruction window.

2 (Withdrawn).    The method of claim 1, said receiving a new store further compromising:

allocating an entry at a tail of a first level store queue;

monitoring said first level store queue, wherein said monitoring includes determining when said first level store queue is full;

determining a previous store from a head of said first level store queue;

determining a subsequent store, wherein said subsequent store needs to be inserted into said instruction window; and

removing said previous store from said head of said first level store queue.

3 (Withdrawn).    The method of claim 1, further comprising:

associating a speculative bit with said checkpoint and a cache block in said

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second level circuit, wherein said speculative bit indicates if said cache block is

speculative or committed.


4 (Withdrawn).       The method of claim 1, further comprising:

    associating a valid bit with said checkpoint and a cache block in said second level

circuit, wherein said valid bit indicates if said cache block is valid or invalid.


5 (Withdrawn).       The method of claim 3, further comprising:

    associating a valid bit with said checkpoint and a cache block in said second level

circuit, wherein said valid bit indicates if said cache block is valid or invalid.


6 (Withdrawn).       The method of claim 5, further comprising:

    squashing said stores associated with said checkpoint in said second level circuit

by clearing said valid bit, wherein said valid bit is valid.


7 (Withdrawn).       The method of claim 5, further comprising:

    committing one or more stores associated with said checkpoint by clearing said

speculative and valid bits in said cache block associated with said checkpoint.


8 (Withdrawn).       The method of claim 5, further comprising:

    accessing said cache block to interpret said speculative and valid bits for

speculative and/or valid states;

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associating one or more of said speculative and valid bits with a cache block; and

tracking changes to said one or more of said speculative and valid bits in said

cache block.

9 (Withdrawn).     The method of claim 8, further comprising:

moving said store from said cache block to provide space for said subsequent

store, when said subsequent store is addressed to said cache block.

10 (Withdrawn).     The method of claim 8, further comprising:

allocating a subsequent cache block when said subsequent store is not addressed

to said cache block;

writing said subsequent store to said subsequent cache block; and

updating said one or more of said first and second bits associated with said

subsequent cache block.

11 (Currently Amended).     An apparatus, comprising:

a queue to store a last n stores; and

a circuit comprising a speculative data cache to receive and store non-retired

stores from said queue, wherein said ~~circuit~~ speculative data cache includes at least one

storage block to be associated with a checkpoint in a program.

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12 (Currently Amended).    The apparatus of claim 11, wherein said ~~circuit~~ queue

further comprises:

      an address matching circuit; and

      a store select circuit, wherein both of said address matching circuit and said store

select circuit forward stores and/or store data to any dependent loads.

13 (Previously Presented).    The apparatus of claim 11, wherein an n-entry buffer stores

said queue, and wherein said n-entry buffer is a circular buffer with head and tail

pointers.

14 (Currently Amended).    The apparatus of claim 11, wherein said circuit further

comprises:

      a memory dependence predictor to store in a non-tagged array one or more store-

distances, wherein said store-distance includes the number of store queue entries between

a load ~~and/or~~ and a forwarding store.

15 (Previously Presented).    The apparatus of claim 11, wherein said circuit further

comprises:

      an unresolved address buffer to determine a program order condition, wherein

said program order condition includes whether one or more non-issued load instructions

are scheduled ahead of one or more associated store instructions.

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16 (Cancelled).

17 (Currently Amended).    A system, comprising:

    a memory to store at least one store operation;

    a processor to retrieve the at least one store operation from the memory, the

processor ~~including logic~~ to execute the at least one store operation and cause a queue to

store a last n stores; and a circuit <u>comprising a speculative data cache</u> to receive and store

non-retired stores from said queue, wherein said ~~circuit~~ <u>speculative data cache</u> includes at

least one storage block to be associated with a checkpoint in a program.

18 (Currently Amended).    The system of claim 17, wherein said ~~circuit~~ <u>queue</u> further

comprises:

    an address matching circuit; and

    a store select circuit, wherein both of said address matching circuit and said store

select circuit forward stores and/or store data to any dependent loads.

19 (Previously Presented).    The system of claim 17, wherein an n-entry buffer stores

said queue, and wherein said n-entry buffer is a circular buffer with head and tail

pointers.

20 (Previously Presented).    The system of claim 17, wherein said circuit further

comprises:

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a memory dependence predictor to store in a non-tagged array one or more store-

distances, wherein said store-distance includes the number of store queue entries between

a load ~~and/or~~ and a forwarding store.

21 (Previously Presented).    The system of claim 17, wherein said circuit further

comprises:

an unresolved address buffer to determine a program order condition, wherein

said program order condition includes whether one or more non-issued load instructions

are scheduled ahead of one or more associated store instructions.

22 (Cancelled).

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